

1      Claim 1.   In a computer which translates instructions from a target  
2      instruction set to a host instruction set, a method for determining  
3      validity of a translation of a target instruction linked to an earlier  
4      translation comprising the steps of:

5      testing a memory address of a target instruction to be executed against a  
6      copy of the memory address of the target instruction from which a  
7      translation of the target instruction was made,  
8      executing the translation if the addresses compare, and  
9      generating an exception if the addresses do not compare.

1      Claim 2   A method as claimed in Claim 1 in which the step of testing  
2      a memory address of a target instruction to be executed against a copy of  
3      the memory address of the target instruction from which a translation of  
4      the target instruction was made is a process separate from the  
5      translation of the target instruction.

1      Claim 3.   A method as claimed in Claim 1 in which the step of testing  
2      a memory address of a target instruction to be executed against a copy of  
3      the memory address of the target instruction from which a translation of  
4      the target instruction was made is included as a part of the translation of  
5      the target instruction.

1      Claim 4.   A method as claimed in Claim 1 which includes an  
2      additional step of copying a memory address of a target instruction when  
3      a translation of the target instruction is made and linked to an earlier  
4      translation.

1      Claim 5.   A method as claimed in Claim 1 which includes additional  
2      steps of copying a memory address of a target instruction when a  
3      translation of the target instruction is made, and  
4      storing the memory address of a target instruction for comparison with a  
5      memory address of a target instruction to be executed.

1      Claim 6.   A method as claimed in Claim 1 which includes the  
2      additional step of executing the translation without testing a memory  
3      address of a target instruction to be executed against a copy of the  
4      memory address of the target instruction from which a translation of the  
5      target instruction was made if testing can be safely eliminated.

1      Claim 7.   A method as claimed in Claim 1 which includes the  
2      additional step of executing the translation without testing a memory  
3      address of a target instruction to be executed against a copy of the  
4      memory address of the target instruction from which a translation of the  
5      target instruction was made if the memory addresses are on the same  
6      memory page.

1      Claim 8.   Computer implemented software means for determining  
2      validity of a translation of a target instruction linked to an earlier  
3      translation in a computer which translates instructions from a target  
4      instruction set to a host instruction set comprising:

5      means for testing a memory address of a target instruction to be  
6      executed against a copy of the memory address of the target instruction  
7      from which a translation of the target instruction was made,  
8      means for executing the translation if the addresses compare, and

9 means for generating an exception if the addresses do not compare.

1 Claim 9. Computer implemented software means as claimed in Claim  
2 8 in which the means for testing a memory address of a target  
3 instruction to be executed against a copy of the memory address of the  
4 target instruction from which a translation of the target instruction was  
5 made includes means separate from the translation of the target  
6 instruction.

1 Claim 10. Computer implemented software means as claimed in Claim  
2 8 in which the means for testing a memory address of a target  
3 instruction to be executed against a copy of the memory address of the  
4 target instruction from which a translation of the target instruction was  
5 made is a part of the translation of the target instruction.

1 Claim 11. Computer implemented software means as claimed in Claim  
2 8 which includes means for copying a memory address of a target  
3 instruction when a translation of the target instruction is made and  
4 linked to an earlier translation.

1 Claim 12. Computer implemented software means as claimed in Claim  
2 8 which includes  
3 means for copying a memory address of a target instruction when a  
4 translation of the target instruction is made, and  
5 means for storing the memory address of a target instruction for  
6 comparison with a memory address of a target instruction to be  
7 executed.

1 Claim 13. Computer implemented software means as claimed in Claim  
2 8 which includes means for executing the translation without testing a  
3 memory address of a target instruction to be executed against a copy of  
4 the memory address of the target instruction from which a translation of  
5 the target instruction was made if the test can be safely eliminated.

1 Claim 14. Computer implemented software means as claimed in Claim  
2 8 which includes means for executing the translation without testing a  
3 memory address of a target instruction to be executed against a copy of  
4 the memory address of the target instruction from which a translation of  
5 the target instruction was made if the memory addresses are on the  
6 same memory page.

*add*  
*A1*  
*add B7*